ABSTRACT OF THE DISCLOSURE

A power switching circuit including an MOS power switching transistor (P1) is disclosed. The power switching transistor (P1) has a body node that is selectably biased to either its source or its drain, depending upon a comparison of the voltage at the circuit input (IN) relative to the voltage at the circuit output (OUT). In a reverse voltage situation in which the output voltage exceeds the input voltage, a first body node switching transistor (P11) connected between the body node of the power switching transistor (P1) and its source is turned off by a voltage corresponding to the output voltage, as conducted from the drain of the power switching transistor (P1) through a pull-down device (P5) in an inverter. Also in this reverse voltage situation, the gate of the power switching transistor (P1) is isolated from a control input (ON_/OFF) by series pass transistors (N0, N1; P12, P13), and the power switching transistor (P1) is held off by a bias transistor (P10), with a gate voltage also corresponding to the output voltage.